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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/749,674	KAO ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2000 and 14 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *1,2,6, and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-9 have been examined.

Papers Received

2. Receipt is acknowledged of Information Disclosure Statement and Change of Address papers submitted, where the papers have been placed of record in the file.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Execution of Multiple Instruction Sets by Translating Instruction Sets Identified by an Instruction Set Indicator Into a Primary Instruction Word via a Predecode Unit.

4. The disclosure is objected to because of the following informalities: there are many grammatical errors throughout the disclosure. An example of this is on page 4, lines 19-21, where it reads, "responsive to the instruction set selector to modify the value of the program counter to fit the length of the instruction word different from the primary instruction word." The sentence structure renders the statement unclear as to what is meant. Another example is on page 8, line 24. The alternative word "or" cannot be used in this context if both instruction words are wanted to be shown as stored simultaneously. These are just examples and the examiner expects that all other grammatical errors will be corrected as well.

Appropriate correction is required.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 150, 160, 212, 217, 219, 275, 282, 292, and 512. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claim 1 recites the limitation "to modify the value of the program counter to fit the length of the instruction word different from the primary instruction word" in lines 18-20. This limitation is unclear and can be interpreted in multiple ways. The examiner is taking the phrase to mean that the program counter adopts different increment steps depending on the length of the instruction words in the instruction set as stated in the Jagger reference referred to in the background section of the disclosure.

7. Claim 2 is objected to because of the following informalities: line 22 describes "two parts of bits." This can be interpreted as meaning that each bit itself has two parts, which is not possible. The examiner is interpreting the phrase to mean "two sets of bits" to show two different fields of bits in each register. Also, line 24 says that "the other bits stored in the data register is viewed." The word "is" implies reference to the register when the examiner is interpreting the reference to be the bits of the registers, thus, the word "is" must be changed to "are."

8. Claim 6 is objected to because of the following informalities: the phrase "the output of the predecoder is the primary instruction word" of line 9 appears to be redundant. Claim 1 has already shown that the output is such.

9. Claim 7 is objected to because of the following informalities: line 11 shows "a recognized bit" as being part of the Icache. There is no reference to a "recognized bit" in the specification or claims. Therefore, the examiner is taking the phrase to simply mean a bit of some sort that can be recognized by a part of the processor.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1 - 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claim 1 recites the limitation "the status of the processor core" in line 10. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking the claim to mean "a status of the processor core."

13. Claim 2 recites the limitation "the data register" in line 24. There is insufficient antecedent basis for this limitation in the claim. There is a plurality of data registers defined and it is unclear to which one is being referred. The examiner is taking the article "the" to actually mean "each" in order to apply the properties of the bits to each register.

14. Claim 3 recites the limitation "the instruction set" in line 2. There is insufficient antecedent basis for this limitation in the claim. There are multiple instructions sets of mention in the parent claims and it is unclear which is being referenced. The examiner is taking the phrase to mean "an instruction set."

15. Claim 6 recites the limitation "the sub-decoder switching" in line 8. There is insufficient antecedent basis for this limitation in the claim. A sub-decoder is described in claim 5 and thus the examiner is taking the claim to refer to claim 5 as its parent instead of one so that the definition of the sub-decoder may be realized in the current claim. Then, there is no prior reference to a switching function of the sub-decoder in the claims or specification, only a translating function. The examiner is taking this "switching" to actually mean "translating" in order to remain consistent with the new parent claim 5.

Claim Rejections - 35 USC § 102

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. Claims 1, 5, 6, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hammond.

18. In regard to claim 1, Hammond discloses a data processing apparatus for executing multiple instruction sets comprising:

a. a memory, for storing a plurality of instruction words of the instruction sets (figure 5, memory);

b. a processor core, for executing a primary instruction word of the instruction words (figure 5, element 104);

c. a program counter register (PC), for addressing a next instruction word stored in the memory; It is inherent that the processor has a program counter to address a next instruction word stored in memory.

d. a plurality of data registers, for storing data of the instruction words; Column 4, lines 10-15 show registers that hold data manipulated by the computer and thus used by the instructions.

e. a processor status register for storing the status of the processor core, wherein the processor status register contains an instruction set selector (ISS) for indicating a current instruction set of the instruction sets; Column 14, line 63 – column 15, line 6 shows a signal from the decoder that indicates the instruction set so that the demultiplexer selects the correct path. Thus this signal is an instruction set selector. Column 15, lines 41-52, show that this signal (instruction set selector) is changed based on two jump instructions, or switch instructions. It can be seen throughout Hammond that such instructions are the only way to change this signal. Thus, the ISS must be stored so that the demultiplexer can select the appropriate path for the instructions following such a switch instruction. Since the signal shows the current instruction set it is a processor status and the means for which it is stored in can be called a processor status register.

Therefore, the instruction set selector, for indicating a current instruction set, is stored in a process status register.

f. a predecoder (figure 5, elements 540 and 541) for translating at least one of the instruction sets to the primary instruction word and outputting therewith; Column 14, lines 18-20, show that the translator, translates one set of instructions into another set of instructions. Lines 21-29 then go on to show that the new translated instruction set is decoded and executed by the processor and is thus the primary instruction word. The demultiplexer is shown to choose the correct path for the instruction set based on whether it already is the primary instruction word or not.

g. An Icache, for storing the primary instruction word (figure 5, element 542). Since the predecoder outputs the primary instruction word, the Icache stores the primary instruction word.

h. a decoder (figure 5, element 543), for decoding the primary instruction word, wherein the processor core is used for executing the word decoded by the decoder; A shown above, the Icache stores the primary instruction word and since the decoder receives its data from the Icache, it decodes this primary instruction word.

i. a program counter control responsive to the instruction set selector to modify the value of the program counter to fit the length of the instruction word different from the primary instruction word; As stated above, the examiner is taking this statement to mean that the value of program counter is modified by a

different value based upon the instruction set length in order to address the next instruction. It is inherent that the program counter has some sort of control to increment the value to point to the next instruction. If the instruction set changes between 32 and 64 bit instructions (as Hammond's disclosure does) in order to address the next instruction, the amount which the program counter is incremented by must change to fit the size of the instruction. Since the instruction set selector described above shows the current instruction set, this value must be used to indicate to the control what program counter increment value to use.

j. a bus, being an interface between the predecoder and the memory (figure 5, path from memory to element 540).

19. In regard to claim 5, Hammond discloses the apparatus of claim 1, as described above, wherein the predecoder contains at least one sub-decoder, for translating at least one of the instruction sets to the primary instruction word. Since as shown above the translator portion of the predecoder translates an instruction set into the primary instruction word, this translator is in fact a sub-decoder.

20. In regard to claim 6, Hammond discloses the apparatus of claim 5, as described above, wherein the sub-decoder switching is controlled by the ISS and the output of the predecoder is the primary instruction word. As described above the switching is being interpreted as translating. Also as described above, the predecoder output is the primary instruction word. Figure 5 shows that the demultiplexer of the predecoder, is

controlled by the ISS. Thus the sub-decoder is also controlled by the ISS since it selects whether the sub-decoder is activated or not.

21. In regard to claim 8, Hammond discloses the apparatus of claim 1, wherein the instruction set selector includes at least one bit. The instruction set selector is shown by Hammond to be one signal or a second signal (column 15, lines 2-6), or one set of bits or a second set of bits. Thus the instruction set selector must include at least one bit.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond in view of Jaggar (5,568,646) and further in view of Hennessy.

24. In regard to claim 2,

a. Hammond discloses the apparatus of claim 1, as described above;

b. Hammond does not disclose wherein there are two parts of bits in each of the data registers, at least one bit is viewed as an instruction set selection bit (IS) and the other bits stored in the data register is viewed as a target address (TA).

c. Jaggar has shown in figure 1 and column 3, lines 37-52, a plurality of data registers for that include an instruction set flag (instruction set selection bit). This flag, depending on which register it is located in, indicates the instruction set

used by the processor for decoding currently and for past instructions. Hennessy has shown on pages 151-152 the description and illustration of register addressing for branch instructions. This means that a branch instruction branches to an address stored in a register. If one combines these two concepts, the result is a set of registers that indicate an instruction set and hold an address for branching.

d. Jaggar has shown in column 3, lines 44-50, that the instruction set flag can be used for quick exception handling since previous flags are saved. By branching to an address stored in a register, the range of addresses accessible becomes larger as can be seen by figure 3.17 in Hennessy. The ability to recover quickly from exceptions and to have a greater range of addresses for branching would have motivated one of ordinary skill in the art to modify the invention of Hammond to include the instruction selection bits in each data register as taught by Jaggar and to branch to addresses stored in the registers as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art to modify the design of Hammond to include the instruction set selection bits given by Jaggar and the register addressing mode for branching taught by Hennessy so that quick exception handling was achieved while being able to access a wide range of instruction memory through branching.

25. In regard to claim 3, Hammond in view of Jaggar and further in view of Hennessy discloses the apparatus of claim 2, as described above, wherein the target address is a

starting address of the instruction set. Hammond shows in column 5, lines 2-8 that the jump address, or branch address, is the beginning of a set of instructions. Figure 2 shows instructions 211, to be of the new instruction set.

26. In regard to claim 4, Hammond in view of Jaggar and further in view of Hennessy discloses the apparatus of claim 2, as described above, wherein the ISS is set by a specified branch instruction according to the IS in the data registers. The instruction set selector is set on a jump (branch) instruction as shown above. The instruction set will then be in accord with the IS in the current data register, which stores the instruction set of the current instruction as shown above.

27. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond in view of Hennessy.

28. In regard to claim 7,

a. Hammond discloses the apparatus of claim 1, as described above, wherein the bit width of the primary instruction word is not equal to other instruction words. As shown by Hammond (column 15, lines 41-52), the primary instruction word, which requires no translation, is 64-bits and the other instruction word is 32-bits (x86 instructions). Thus the 32-bit word does not have the same bit width as the primary word.

b. Hammond does not disclose that the Icache adds a recognized bit and translates the PC value to point out a relative primary instruction word. Hammond does disclose that the cache holds the relative primary instruction words, but, not that they are pointed out by a PC translation.

c. Hennessy has disclosed an Icache that translates the PC value to point out a relative primary instruction word. Page 552 under number 1 shows that the address comes from the PC. Then, page 554, again under number 1, shows that the cache is indexed using bits 15-2 of the address (PC value). Thus the PC value is translated (by using only a part of the address) to point out a relative primary instruction word (contents of the cache as shown above). The figure of the cache on page 553 shows a valid bit, which is recognized to indicate whether the data is valid or not.

d. This translation allows for multiple cache entries to exist in the cache using only a relative portion of the entire PC, thus saving hardware space and money. The valid bit allows for data integrity to be realized. The ability to save hardware space and cost while ensuring data integrity would have motivated one of ordinary skill in the art to modify the design of Hammond to include the cache circuitry disclosed by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Hammond to include the cache logic disclosed by Hennessy so that system hardware space and cost is saved and data integrity is introduced.

29. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond in view Jaggar.

30. In regard to claim 9,

a. Hammond discloses the apparatus of claim 1, as described above;

b. Hammond does not disclose that the instruction set selector can be set according to one or more instruction set bits of the data registers.

c. Jaggar has shown in figure 1 and column 3, lines 37-52, a plurality of data registers for that include an instruction set flag (instruction set selection bit). This flag, depending on which register it is located in, indicates the instruction set used by the processor for the current and past instructions. Therefore, when Jaggar sets the instruction set selector as shown above on a specified jump (branch) instruction, the instruction set selector is being set in accordance with the instruction set selection bit of the data registers.

d. Jaggar has shown in column 3, lines 44-50, that the instruction set flag can be used for quick exception handling since previous flags are saved. The ability to recover quickly from exceptions would have motivated one of ordinary skill in the art to modify the invention of Hammond to include the instruction selection bits in each data register as taught by Jaggar.

It would have been obvious to one of ordinary skill in the art to modify the design of Hammond to include the instruction set selection bits given by Jaggar so that quick exception handling was achieved.

Conclusion

31. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are disclosed to further show the art with respect to multiple instruction set decoding and execution in general.

US Pat No 5,115,500 to Larsen shows the use of instruction set selection bits in registers.

US Pat No 6,101,592 to Pechanek shows translation of an instruction subset to.

US Pat No 5,598,546 to Blomgren shows a system for executing RISC and CISC instructions where the switching is performed by a branch or jump instruction.

US Pat No 5,481,684 to Richter shows execution of both RISC and CISC instructions with a descriptor indicating the instruction set.

US Pat No 6,021,484 to Park shows the translation of one instruction set to another using a predecoder for ready decoding and execution.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7035. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Shane F Gerstl
Examiner
Art Unit 2183

SFG
November 17, 2003

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